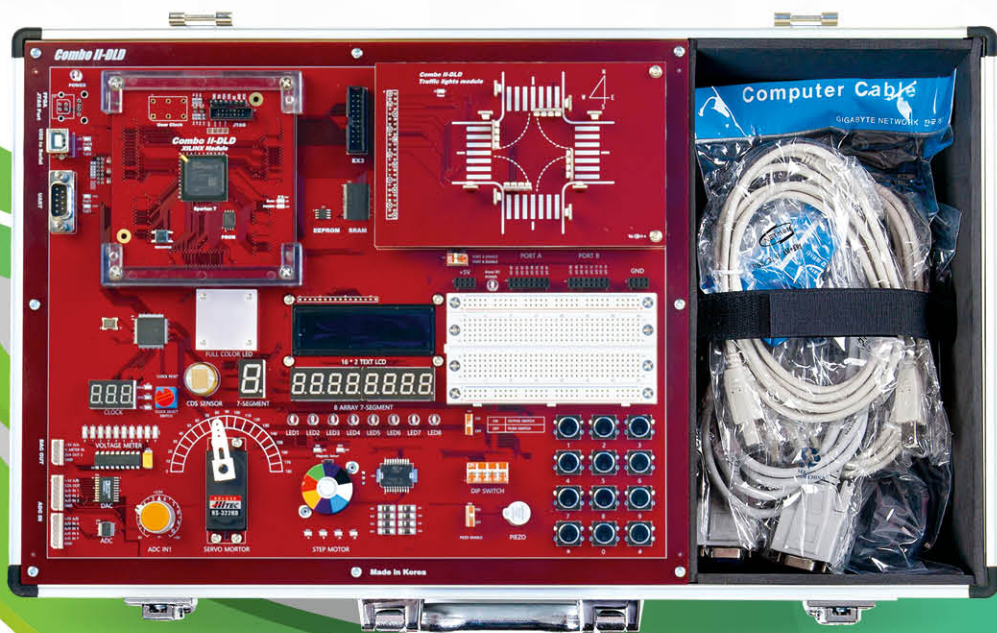


ALTERA AMD based

# FPGA Digital Circuit Design Trainer

## COMBO II DLD



HANBACK ELECTRONICS CO.,LTD.

518 Yuseong-daero, Yuseong-Gu, Daejeon 34202, South Korea  
TEL. +82-42-610-1111, 1164 (Dir.)  
FAX. 042. 610. 1199  
E mail. support@hanback.co.kr



Homepage

ALTERA AMD based

## FPGA Digital Circuit Design Trainer

# COMBO II DLD

Considering the flexibility and scalability of FPGA device, we modularized to enable replacement use of ALTERA and AMD devices

Download cables for ALTERA and AMD are provided for USB, making it easier to use in any PC environment

With the Bread Board installed as standard, the user can configure TTL circuit and experiment

16 types of clocks between 1 Hz and 50 MHz using Clock Control Block and the clock generator installed by the user on the FPGA module can be selected and used for purpose

Provides educational themes that organizes the theory and practice of digital logic circuits by subject, making it easier to understand the logic circuits in general

### Training Contents

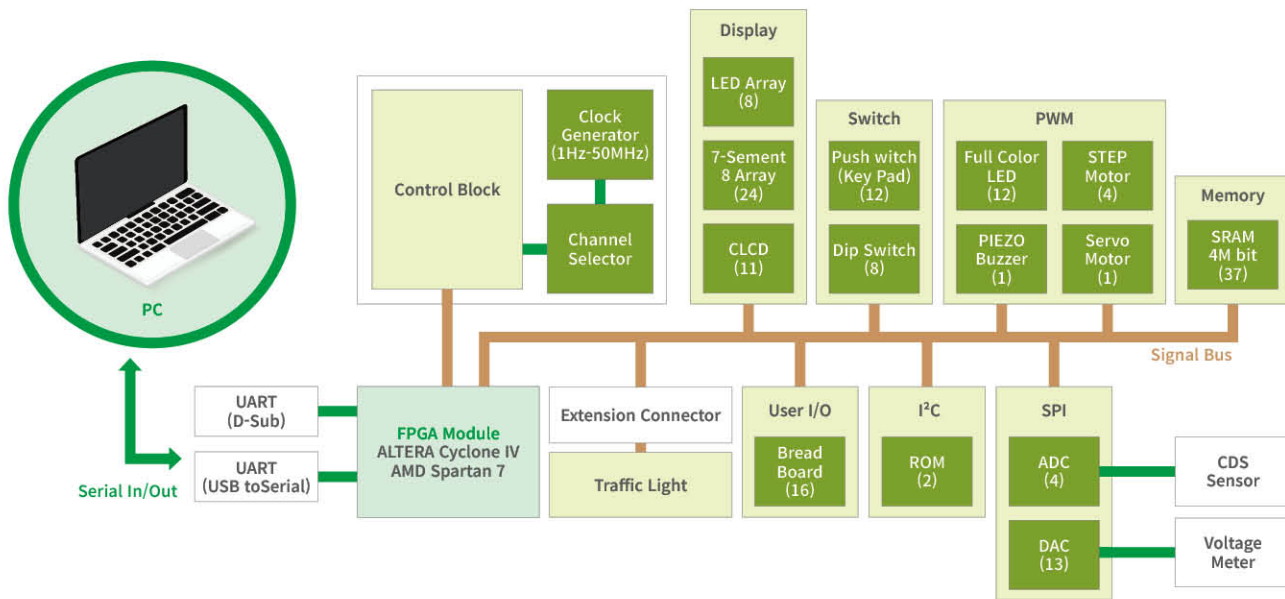
#### DIGITAL DESIGN BASICS AND PRACTICE PREPARATION

#### FPGA DIGITAL LOGIC DESIGN

- |  |  |
|--|--|
| 1. TRAINING EQUIPMENT (COMBO II DLD)             | 2.5. Clock and Sequence Logic Circuit                      |
| 2. DIGITAL LOGIC CIRCUIT DESIGN                  | 2.6. Application of Clock and Counter Circuit              |
| 2.1. Logic Gate Implementation                   | 2.7. Implementation of PWM(Pulse Width Modulation) Circuit |
| 2.2. Basic Combinational Logic Circuit Design    | 2.8. Register  |
| 2.3. Advanced Combinational Logic Circuit Design | 2.9. Implementation of State Machine                       |
| 2.4. Arithmetic Circuit Design                   |  |

#### APPLIED DIGITAL LOGIC CIRCUIT DESIGN

- |                                       |   |
|---------------------------------------|---|
| 3.1. Character LCD Control            | 3.4. DAC and ADC                          |
| 3.2. Serial Communication using RS232 | 3.5. Expansion Application-Traffic Signal |
| 3.3. Control External Memory (SRAM)   |   |



## Design Environment

List	Specifications
ALTERA Module	Quartus Prime Lite Edition
AMD Module	Vivado

## Hardware Specification

List	Specifications
FPGA Device	ALTERA Cyclone IV Series (EP4CE30F, EP4CE40F) AMD Spartan 7 Device(XC7S75)
Clock Control	1 Hz ~ 50MHz Changeable Clock
Memory	4Mbit SRAM, 16kB 2Wire Serial EEPROM
Display	Text LCD, 8 Array LED, 4 Cell Full Color LED, 7-Segment, 8 Array 7-Segment
Actuator	1EA Servo Motor, 1EA Step Motor
AD/DA	SPI ADC : 1 Channel 8Bit 1MHz Sampling, Parallel DAC : Dual Voltage Output 8-Bit DAC
Sensor	CdS, Voltage Meter (LED)
Etc	PIEZO, Bread Board, Dip Switch, Push Switch
UART	2 Channel UART (USB to Serial 1 Port , D-Sub 9 Pin 1 Port )
Extension Connector	2EA 50pin Connector (FPGA I/O 84Pin)
Project Module	Traffic Light Module
Option Module	Vending Machine Module

# Layout

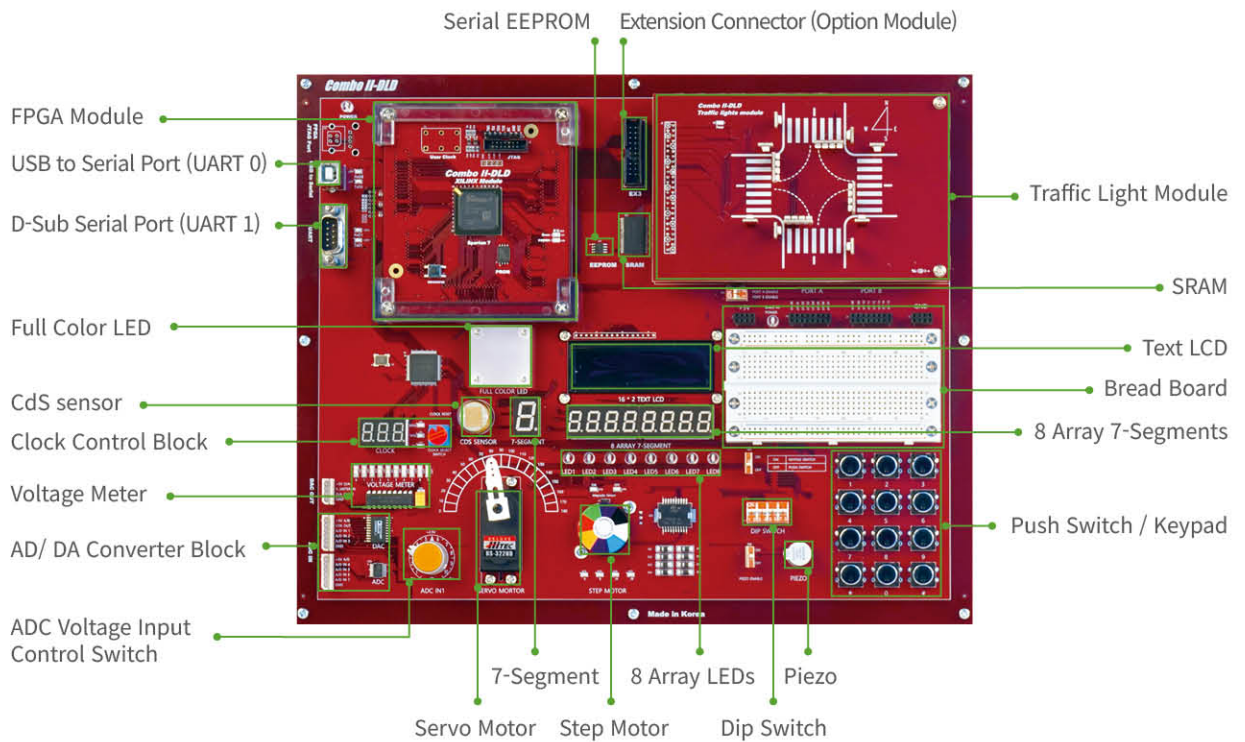


ALTERA

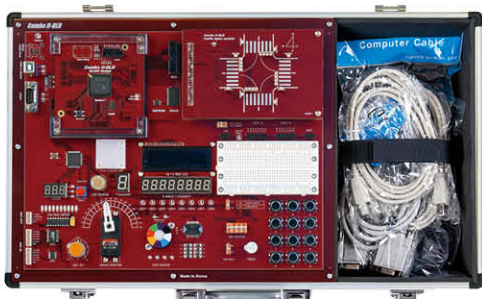


AMD

- ALTERA module and AMD module selectively available
- Provides systematic training content of Digital Logic Design
- You can select 16-input frequencies with Clock Control Block
- ALTERA : Cyclone IV Series applied  
AMD : Spartan 7 Series applied
- Provides experimental practice themes through a variety of optional modules



# Components



Combo II DLD



AC Power Cable



USB Cable (A to B Type)



Platform USB



Serial Cable



USB Programmer



User Guide book